H·A

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,466	10/03/2003	Shau-Lim Stan Chow	00005-014	3348

7590 04/15/2005

Anthony T. Cascio
Suite 314
423 Broadway Ave.
Millbrae, CA 94030-1905

EXAMINER	
SIEK, VUTHE	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/678,466	CHOW ET AL.
	Examiner	Art Unit
	Vuthe Siek	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-11,13,15,18-21,23-28,30,32 and 35* is/are rejected.

7)☒ Claim(s) *5,12,14,16,17,22,29,31,33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/678,466 filed on 10/3/2003. Claims 1-35 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6-11, 13, 18-21, 23-28, 30 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Dahl et al. (6,865,721).

4. As to claims 1 and 18, Dahl et al. teach a method pin assignment in a block in a block-based integrated circuit design process (Fig. 1-8, 9B, 10-17, summary), the method comprising steps of assigning within the block a plurality of block pins to a respective one of a plurality of first locations (assigning pins/ports within each of the blocks 10-30, 60-94 of Fig. 3, at least in col. 7); placing in the block a plurality of components wherein each of the components is placed relatively proximal to the pins respectively connecting to each of the components (using a software tool to perform placing and routing, press operation and optimization of each block separately based on each block netlist, Fig. 9B, 8, 10-12); moving selected ones of the pins to a respective one of second locations proximal the components connecting to the selected ones of

the pins (Fig. 9B, 8, 10-12; col. 9-10); and refining placement of the components with respect to the selected ones of the pins at the second location connecting thereto (Fig. 9B-12; col. 9-10, a software tool perform placement, routing, optimization, and press operation).

5. As to claims 2 and 19, Dahl et al. teach pin assignment includes locating the first locations proximal a periphery of the block; and placing the pins in the first locations in accordance with connectivity constraints to other such pins connecting thereto contained in other such blocks at a current hierarchical level of the integrated circuit (Fig. 9B, 10-11, where Fig. 11C shown optimization of placement associated with pin assignment of block-level placement, connectivity as much shorter compared to Fig. 10C; col.9-10 and Fig. 12-16 shown pin assignment in hierarchical physical design process).

6. As to claims 3 and 20, Dahl et al. teach wherein said placing step is performed using a heuristic based on a shortest distance of each of the pins in the block to pins in other such blocks to which each of the pin connects (Fig. 9B, 10-11, where Fig. 11C shown optimization of placement associated with pin assignment of block-level placement, connectivity as much shorter compared to Fig. 10C; col.9-10).

7. As to claims 4 and 21, Dahl et al. teach wherein global routing to detect blockages and congestion is used to avoid the blockages and congestion while routing a connection from each of the pins to the pins in the other blocks (Fig. 9B, col. 9-10).

8. As to claims 6 and 23, Dahl et al. teach wherein said placing step includes the step of maintaining parallel alignment of bus pins in the block to corresponding bus pins

in one other of the blocks, wherein the bus pins in the block and the one other of the blocks are each abstracted as a single distributed pin (Fig. 9B, 3, 8, 11C, 12B, 12C, 14 shown pin alignment between blocks).

9. As to claims 7 and 24, Dahl et al. teach defining a bounding box containing a plurality of component pins of selected ones of the components to which a respective one of the block pins connects; and distributing each respective one of the block pins into the bounding box containing the component pins to which it connects (Fig. 13, where each bounding box of each block is optimized separately, including moving pins or relocating pin to position where closely connected to component pins or ports within each block as shown in Fig. 11C, where connections are shorter as compared to Fig. 10C, see also col. 7, where placement, routing and optimization are performed within each block, where pins within the block are free to be relocated).

10. As to claims 8 and 25, Dahl et al. teach wherein said distributing step and said refining step are reiteratively performed (a software tool perform placement, routing, press operation and optimization based on abutted-pin hierarchical physical design, Fig. 9B, col. 9).

11. As to claims 9 and 26, Dahl et al. teach moving step includes the step of abstracting a shape of each of the pins from a small shape to a distributed shape to enhance routability at a top hierarchical level of the integrated circuit (Fig. 9B, col. 9; Dahl teaches power/ground/signal lines, pins, ports associated to a variety of components, therefore pins having different shapes that are adapted to be suitable to these different lines, col. 7). Top-level components having different types (explicitly

having different shapes of pins assigned) are placed and routed at the top-level and then press into block-level, where placement, routing and optimization are performed separately within individual blocks (col. 7).

12. As to claims 10 and 27, Dahl et al. teach wherein the block has a plurality of metal layers, the pins being in a selected one of the metal layers (col. 9, routing metal for each block where each block having components and pins).

13. As to claims 11, 13, 28 and 30 Dahl et al. using a software to press top-level components into block-level (lower level) as shown in Fig. 3 as exemplary, where each block is separately placed, routed and optimized separately based on abutted-pin hierarchical physical. Accordingly, the width of the pins must be substantially equivalent to a minimum layer width of the selected one of the metal layers because the top level is collapsed or merged or pressed into low-level.

14. As to claim 35, Dahl et al. teach performing assigning, placing, moving and refining (optimizing) on each of the blocks sequentially with respect to each other of the blocks at the current hierarchical level in the netlist (at least col. 7).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 15 and 32 are rejected under 35 U.S.C. 103(a) as being obvious over Dahl et al. (6,865,721) in view of Ho (6,734,472).

17. As to claims 15 and 32, Dahl et al. routing power and ground nets and signal nets. Dahl et al. do not teach interposing one of power net and ground net between signal nets. Ho teaches the claimed limitation at least in Fig. 3-4 in order to remove both capacitive and inductive signal coupling effects of the routing in IC chips (col. 4, lines 11-16, summary). Incorporating the teachings of Ho into Dahl would be obvious to one practitioners in the art at the time the invention was made in order to reduce the capacitive and inductive signal coupling effects of the routing resources of and IC design.

Allowable Subject Matter

18. Claims 5, 12, 14, 16-17, 22, 29, 31 and 33-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The prior art of record does not teach or fairly suggest the limitation of claims 5 and 22, wherein said placing step includes the step of selecting from a criticality ranking associated with each of the timing paths a most critical timing path between the block and one other of such blocks such that the pins on the most critical path are first assigned and pins on remaining timing paths assigned in order of decreasing criticality ranking.

20. As to claims 12 and 29, the prior art of record does not teach or fairly suggest wherein the width of one of the pins is a width of a net to which the one of the pins is contained in the event the width of the net is required to be larger than the minimum layer width.

21. As to claims 14 and 31, the prior art of record does not teach or fairly suggest wherein the spacing between two selected ones of the pins is larger than the minimum layer spacing for the selected one of the layers in the event a net containing the two selected ones of the pins requires a larger spacing than the minimum spacing.

22. As to claims16-17 and 33-34, the prior art of record does not teach or fairly suggest defining a virtual pin to a selected location in a temporary top metal layer of the block; routing between the virtual pin and a further pin in a lower metal layer within the block wherein at least one via is formed between the temporary top layer and a lower metal layer immediately below the temporary layer; and abstracting the block wherein the top metal layer and the via are removed, one of the pins being assigned in the second metal layer to the selected location immediately below the removed via.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER